CLAIMS

Please **AMEND** claim 11 as follows:

Please **CANCEL** claims 14-19 as follows:

A status of the claims is provided below.

1. (original) A method for manufacturing an integrated circuit comprising a plurality of semiconductor devices including an n-type transistor and a p-type transistor, the method comprising:

depositing oxide fill on the n-type transistor and the p-type transistor and chemical/mechanical polishing the deposited oxide fill such that a gate stack of the n-type transistor and a gate stack of the p-type transistor, the n-type transistor and the p-type transistor each having spacers are surrounded with oxide,

etching a portion of the polysilicon from a gate of the p-type transistor;

depositing a low-resistance material on the p-type transistor and the n-type transistor; and

heating the integrated circuit such that the deposited low-resistance material reacts with the polysilicon of the p-type transistor and the polysilicon of the n-type transistor, such that compressive mechanical stresses are formed along a longitudinal direction of a channel of the p-type transistor.

2. (original) The method of claim 1, further comprising removing a portion of the deposited low resistance material.

3. (original) The method of claim 1, further comprising:

covering an n-type transistor with a mask prior to performing the step of etching; and

removing the mask after performing the step of etching.

4. (original) The method of claim 3, wherein the mask is a patterned photoresist layer.

5. (original) The method of claim 1, wherein the step of depositing comprises depositing at least one of Co, HF, Mo, Ni, Pd_2, Pt, Ta, Ti, W, and Zr on the p-type transistor and then n-type transistor.

6. (original) The method of claim 2, wherein the step of removing comprises removing a portion of the deposited low-resistance material with a selective etching technique.

7. (original) The method of claim 1, wherein the step of heating comprises heating the integrated circuit to a temperature of about 300°C to about 1000°C.

8. (original) The method of claim 1, wherein the step of depositing a low-resistance material comprises depositing a low-resistance material to a height of approximately 30Å -200 Å.

9. (original) The method of claim 1, wherein the step of etching a portion of the polysilicon comprises etching about half of the polysilicon from the p-type transistor.

10. (original) The method of claim 1, wherein the step of etching comprises etching the polysilicon from the gate of the p-type transistor such that a n-type polysilicon to p-type polysilicon ratio is about 2:1.

11. (currently amended) The method of claim 1, wherein the etching comprises etching about 250 to about 750Å of the p-type polysilicon.

12. (original) The method of claim 1, wherein the step of etching comprises etching the polysilicon from the gate of the p-type transistor using a wet etch or a dry etch.

13. (original) The method of claim 1, wherein the step of depositing a low-resistance material comprises depositing a low resistance material on the p-type transistor and the n-type transistor using evaporation, sputtering or chemical vapor deposition techniques.

14-19 (cancelled).

20. (original) A method for manufacturing an integrated circuit comprising a plurality of semiconductor devices including an n-type transistor and a p-type transistor, the method comprising:

forming a polysilicon layer on the n-type transistor and the p-type transistor, wherein the polysilicon layer on the p-type transistor has a shorter height than the polysilicon layer on the n-type transistor;

depositing a low-resistance material on the p-type transistor and the n-type transistor; and

heating the integrated circuit such that the deposited low-resistance material reacts with the polysilicon of the p-type transistor and the polysilicon of the n-type transistor, such that compressive mechanical stresses are formed along a longitudinal direction of a channel of the p-type transistor.